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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,271	12/31/2003	Do-young Kim	249/430	6611

7590 10/17/2005

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EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/748,271	KIM ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 67-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 67-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: "200 Brinell" recited in claims 3 and 12 must be described in the originally field disclosure.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-19 and 67-70 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1-19 and 67-70, the recitation, "a thin film semiconductor device includes a semiconductor chip" is not proper since a semiconductor chip is more complete than a thin film semiconductor device. The thin film semiconductor device is only part of a semiconductor chip. The preamble should be corrected to read "a semiconductor chip". Further, regarding claims 6 and 15, a thin film transistor, a thin film diode, and a metal insulator metal are not semiconductor chips. They are semiconductor devices.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 6, 10, 13, 15, 19 and 67-68 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (US 2005/0205868).

Regarding claim 1, Yamazaki et al. discloses in figures 3-4 (showing the manufacturing step of Embodiment 1), particularly in figure 4D a thin film semiconductor device comprising a flexible substrate 301 (figure 3A); a semiconductor chip NTFT, which is formed on the flexible substrate; a protective cap 330 (para [0142], lines 1-2) which seals the semiconductor chip; and an insulating region 331 (para [0142], line 6) formed on the protective cap.

Note that substrate 301 is formed of glass (para [0106], line 2), which is the same material being used to form the flexible substrate in the instant application (para [0012] of the instant application). As such substrate 301 is "flexible". Further, element 330 constitutes a similar structure as the claimed protective cap and therefore is capable of performing as a protective cap.

Regarding claim 4, Yamazaki et al. discloses in figure 4D the protective cap 330 is formed on an upper surface of the semiconductor device.

Regarding claim 6, Yamazaki et al. discloses in figure 4D the semiconductor chip NTFT is a thin film transistor.

Regarding claim 10, Yamazaki et al. discloses in figures 3-4 (showing the manufacturing step of Embodiment 1), particularly in figure 4D an electronic device including a flexible substrate 301 and a semiconductor chip NTFT formed on the flexible substrate, the electronic device comprising a protective cap 330 that seals the semiconductor chip and an insulating region 331 formed on the protective cap.

Regarding claim 13, Yamazaki et al. discloses in figure 4D the protective cap 330 is formed on an upper surface of the semiconductor chip NTFT.

Regarding claim 15, Yamazaki et al. discloses in figure 4D the semiconductor chip NTFT is a thin film transistor.

Regarding claim 19, Yamazaki et al. discloses in para [0257] an LCD connected to the semiconductor chip.

Regarding claim 67, Yamazaki et al. discloses in figures 3-4 (showing the manufacturing step of Embodiment 1), particularly in figure 4D the semiconductor chip comprises an active semiconductor element formed on the flexible substrate, the active semiconductor element including a source, a drain and a channel (NTFT inherently constitutes all these elements); an insulating region 305 (para [0114], line 1) formed on the active semiconductor element; a gate electrode 306 (para [0114], lines 3-4) formed on the insulating region; a second insulating region 326 (para [0140], line 1) formed on

the gate electrode; a source electrode 327 (para [0140], line 2) formed on the second insulating region and connected with the source; a drain electrode 329 (para [0140], line 2) formed on the second insulating region and connected with the drain, and wherein the protective cap 330 is formed on the second insulating region and on the source and drain electrodes.

Regarding claim 68, Yamazaki et al. discloses in figure 26 the structure (CMOS) as shown in figures 3-4 being incorporated to form a display device, showing a third insulating region 4142 (para [0344], lie 3) formed on the protective cap; a first pixel electrode 4143 (para [0345], line 1) formed on the third insulating region; a pixel element (para [0346], line 3) formed on the first pixel electrode; and a second pixel electrode 4146 (para [0352], line 5) formed on the pixel element.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3, 7-8, 11-12 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. in view of Ikeda et al. (US 2002/0036267).

Regarding claims 2-3, 7, 11-12 and 16, applicant teaches in para [0051] and [0052] the protective cap formed of an ultraviolet curing material (acrylic resin) has a

tensile strength higher than about 30 GPa and a hardness higher than about 200 Brinell. Yamazaki et al. discloses the protective cap 330 is formed of silicon nitride (para [0142], line 2). Yamazaki et al. does not disclose the protective cap is formed of acrylic resin. However, Ikeda et al. discloses the protective cap 107 can be formed of silicon nitride or acrylic resin (para [0086], lines 1-5). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamazaki et al. by having the protective cap formed of an ultraviolet curing resin because silicon nitride and acrylic resin are recognized in the art as equivalents, and therefore, the protective cap formed of acrylic resin inherently has a tensile strength higher than about 30 GPa and a hardness higher than about 200 Brinell.

Regarding claim 8 and 17, Ikeda et al. discloses the flexible substrate is formed of plastic (para 0083], lines 8-9).

Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al.

Regarding claims 9 and 18, Yamazaki et al. discloses in figure 3A the flexible substrate 301 is a glass substrate (para [0106], line 2). Yamazaki et al. does not disclose a thickness of the glass substrate being less than about 100 μm. However, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify Yamazaki et al. by having a thickness of the glass substrate being less than about 100 μm, since it has been held that discovering an

optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Claims 5, 14, 69 and 71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al in view of Asano et al. (US 6,916,681).

Regarding claims 5 and 14, Yamazaki et al. discloses in figure 4D the protective cap 330 is formed on an upper surface of the semiconductor chip. Yamazaki et al. does not disclose the protective cap being between the semiconductor chip and the flexible substrate. However, Asano et al. discloses in figure 7 the protective cap 703 (col. 10, line 6. Element 703 is similar to element 603 in figure 6, which functions as a protective layer. Also see col. 9, lines 36-37) being between the semiconductor chip 706 and the flexible substrate 701 (col. 9, lines 63-67). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamazaki et al. by having the protective cap being between the semiconductor chip and the flexible substrate to further protect the semiconductor chip from foreign objects.

Regarding claim 69, similar to claim 5, Yamazaki et al. and Asano together disclose the structure set forth in claim 69.

Regarding claim 71, similar to claims 67 and 69, Yamazaki et al. substantially all the structure set forth in claim 71. Yamazaki et al. further discloses in figure 4D a second region of the protective material 330 is formed on the second insulating region 326 and on the source and drain electrodes 327, 329, and on the portion of the region of the protective material extending laterally beyond the active semiconductor element.

Yamazaki et al. does not disclose an active semiconductor element formed on a region of the protective material and a portion of the region of the protective material extending laterally beyond the active semiconductor elements. However, Asano et al. discloses in figure 6 an active semiconductor element 607, 608 formed on a region of the protective material 603 and a portion of the region of the protective material extending laterally beyond the active semiconductor elements. In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamazaki et al. by having an active semiconductor element formed on a region of the protective material and a portion of the region of the protective material extending laterally beyond the active semiconductor elements to further protect the semiconductor chip from foreign objects.

Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Asano et al. (US 6,916,681) in view of Ikeda et al.

Regarding claim 70, similar to rejection of claims 2 and 11, the combination of Yamazaki et al. and Asano et al. and Ikeda et al. reads on claim 70.

Response to Arguments

Applicant's arguments with respect to claims 1-19 and 67-71 have been considered but are moot in view of the new ground(s) of rejection.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
October 13, 2005.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER